AMENDMENTS TO THE CLAIMS

IN THE CLAIMS:

Claims 17 and 18 are cancelled. Claims 12-16 and 19-20 and new claims 21-27 are currently pending, based on the amendment herein:

12. (Original) A method for making a body contact in a silicon-on-insulator transistor, said method comprising the steps of:

placing a shallow trench isolation on a substrate between regions of an SOI layer;

depositing a gate conductor over a portion of said substrate;

applying a first dummy gate mask over a first portion of said gate conductor;

etching said gate conductor such that said gate conductor not comprising said first portion of said gate conductor is removed;

depositing an insulator on said substrate;

polishing said insulator;

applying a second gate mask over a second portion of said gate conductor;

etching said gate conductor such that said gate conductor not comprising said second portion of said gate conductor is removed;

depositing spacer portions on said substrate such that said spacer portions isolate said second portion of said gate conductor and said insulator from the rest of said transistor;

depositing charged implants in said substrate.

13. (Original) The method of claim 12 wherein said insulator is an oxide.

14. (Original) The method of claim 12 wherein said insulator is a nitride.

15. (Currently Amended) A method of reducing capacitance in a silicon-on-insulator transistor, said transistor having a source region, a drain region, a body-contact region, and a first gate connecting said source region to said drain region, said method comprising the step of isolating said body-contact region from said source region and said drain region by forming a structure comprising an insulator and insulative spacers, said insulator not forming a part of said first gate, and wherein said insulative spacers are in contact with external surfaces of said insulator such that an interior portion of said insulator is between said spacers.

16. (Currently Amended) The method of claim 15 wherein said step of is of isolating said body-contact region is accomplished by replacing a portion of said first gate with ~~an~~ a second gate, wherein said second gate has a thickness that is greater than a thickness of said first gate, said second gate comprising said insulator.

17. (Cancelled)

18. (Cancelled)

19. (Currently Amended) ~~The~~ A method of reducing capacitance in a silicon-on-insulator transistor, said transistor having a source region, a drain region, a body-contact region, and a gate connecting said source region to said drain region, said method comprising the step of isolating said body-contact region from said source region and said drain region, wherein said step of isolating said body-contact region is accomplished by forming, during fabrication, a gap between said body-contact region and said source region and said drain region.

20. (Original) The method of claim 19 wherein said gap is created by preventing the formation of conductive material in a region between said body-contact region and said source region and said drain region.

21. (New) The method of claim 15 wherein said insulator has a lower dielectric constant than said first gate.

22. (New) The method of claim 15 wherein said insulator comprises an isolation material, said isolation material surrounding said semiconductor device.

23. (New) The method of claim 22 wherein said isolation material comprises an STI trench.

24. (New) The method of claim 15 wherein said insulator comprises a layer of insulation with no gate conductor on said insulation.

25. (New) The method of claim 24 wherein said layer of insulation comprises a layer of oxide or nitride.

26. (New) The method of claim 15 wherein said spacers interrupt a continuity of a silicide material.

27. (New) The method of claim 15 further comprising forming a metal layer shorting said body contact to either said source region or said drain region.